REMARKS/ARGUMENTS

The Examiner's final Restriction Request is acknowledged and non-elected claims 6-10 have been canceled. A divisional application will be filed at a later date.

Examiner Michelle Estrada is thanked for thoroughly reviewing the subject application. Examiner is also thanked for allowing claims 1-5. All claims are believed to be in condition for allowance.

Claim Objections

Reconsideration of the rejection of claims 11-31 is respectfully requested based on the following.

The Examiner is thanked for pointing out the various informalities in the claims. The claims have been carefully reviewed and amended to correct those problems the Examiner pointed out. All claims are now believed to be in allowable condition.

In light of the foregoing response, applicant respectfully requests that the Examiner's claim rejection of claims 11-31, be withdrawn.

Claim rejections - 35 U.S.C. § 102

Reconsideration of the rejection of claims 11, 13, 14, 20 and 22 under 35 U.S.C. 102(e) as being anticipated by Wu (U.S. Patent 6,489,237 B1) is respectfully requested based on the following.

Claims 14 and 20 have been amended with the addition of limitation "said semiconductor surface comprising at least one completed semiconductor device, said at least one completed semiconductor device being densely packed and having a relatively large surface area" to the original clause of "providing a semiconductor surface".

This amended limitation has been quoted from the objectives of the invention, as these objectives have been stated on pages 4 and 5 of the specification, no new matter has therefore been introduced.

Claims 13, 14 are dependent claims to claim 11, claim 22 is a dependent claims to claim 20.

Wu provides a method for patterning lines in semiconductor devices. More specifically, Wu provides for:

- a layer 18 of conductive material, as shown in the cross section of Fig. 3, over which a patterned layer 20 of sacrificial silicon oxide having an opening 19, as shown in the cross section of Fig. 4, over which a layer 22 of spacer material and a layer 24 of hardmask material, as shown in the cross section of Fig. 5, polishing the stack of layers down to the layer 22 of spacer material, as shown in the cross section of Fig. 6, leaving the spacer material 24 inside opening 19
- removing the layers 22, of spacer material, and 20, of sacrificial silicon oxide, using the spacer material 24 inside opening 19 as a mask
- removing layer 24 of hardmask material and layer 20, of sacrificial silicon oxide, from the patterned layer 18 of conductive material, having created an ultra-fine layer 18 of conductive interconnect, as shown in the cross section of Fig. 8.

To highlight the differences between the Wu invention and the claimed invention, amended claim 11, which specifies a method of the claimed invention for applying a stress relief interface layer over a semiconductor surface, of the claimed invention is quoted below, underlining in this quote the aspects of the claimed invention that are not provided by the Wu invention, making the claimed invention patentable over the Wu invention, as follows:

- providing a semiconductor surface, the semiconductor surface comprising at least one completed semiconductor device, the at least one completed semiconductor device being densely packed and having a relatively large surface area
- depositing a stress relief **interface layer** over the semiconductor surface, and
- creating at least one opening through the stress relief interface layer.

The above highlighted differences between the Wu invention and the claimed invention are further emphasized by the dependent claims to claim 11, for instance claim 13 specifies that the stress relief interface layer relieves stress introduced by mismatched Coefficients of Thermal Expansion (CTE) of thermally interacting layers, claim 14 specifies that the

stress relief interface layer comprising polysilicon while claim 15 specifies depositing a layer of mold compound over the surface of the stress relief interface layer, filling the at least one opening created through the stress relief interface layer.

The Wu invention therefore does not provide for:

- enhancing adhesion between a layer of stress relieve material and a layer of protective material deposited over the surface of a completed semiconductor device
- reducing stress introduced by a mismatch of the CTE of adjacent layers that are created as protective layers over a completed semiconductor device
- preventing damage to a device package or components thereof that is introduced by thermal or mechanical stress that is created in one or more of the layers of the completed package, and
- providing a method of creating a protective layer over a completed semiconductor device where the completed semiconductor device is densely packed and has a relatively large surface area.

In light of the foregoing response, applicant respectfully requests that the Examiner's rejection of claims 11, 13, 14, 20 and 22 under 35 U.S.C. 102(e) as being anticipated by Wu (U.S. Patent 6,489,237 B1, be withdrawn.

Claim rejections - 35 U.S.C. § 103

Reconsideration of the rejection of claims 12, 15-19, 21 and 23-31 under 35 U.S.C. 103(a) as being unpatentable over Wu (U.S. Patent 6,489,237 B1) as applied to claims 11, 13, 14, 20 and 22 above and further in view of Tokushige et al. (U.S. Patent 6,329,288) is respectfully requested based on the following.

Wu (U.S. Patent 6,489,237 B1) is removed as a reference under 35 U.S.C. 103(a) because the referenced patent, and the claimed invention, were, at the time the invention was made, owned by the same person. Please see the following 103(c) statement.

103(c) Statement

Application 10/058,473 and U.S. Patent 6,489,237 B1 (Wu) were, at the time the invention of Application 10/058,473 was

made, commonly owned by Taiwan Semiconductor Manufacturing Company, Hsinchu, Taiwan.

With the removal of U.S. Patent 6,489,237 B1 (Wu) as a reference under 35 U.S.C. 103(c), the above rejection is now considered moot.

In light of the foregoing response, applicant respectfully requests that the Examiner's rejection of claims 12, 15-19, 21 and 23-31 under 35 U.S.C. 103(a) as being unpatentable over Wu (U.S. Patent 6,489,237 B1) as applied to claims 11, 13, 14, 20 and 22 above and further in view of Tokushige et al. (U.S. Patent 6,329,288), be withdrawn.

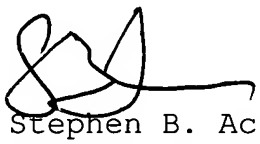
The prior art made of record and not relied upon that is considered pertinent to Applicant's disclosure, that is Koike (U.S. Patent 6,294,454 B1), Shindo et al. (U.S. Patent 5,048,179), Lin et al. (U.S. Patent 6,593,649 B1) and Ho (U.S. Patent 6,277,672 B1) have been examined and have been found to be of general interest to the invention.

Other Considerations

No new independent or dependent claims have been written as a result of this office action, no new charges are therefore incurred due to this office action.

It is requested that, should Examiner not find the claims to be allowable, to call the undersigned Attorney at the Examiner's convenience at 845-452-5863 in order to overcome any problems preventing allowance of the claims.

Respectfully submitted,



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